ASIC Status Report

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for

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ASIC Status

- Prototype production parts under test
- Very flexible prototype chip
  - Multiple modes
    - Continuous Muxed output (BASELINE)
      - External Quad 12bit 40MS/s ADC
    - SCA Mode
      - 64 sample capacitors per channel, depth 32us
      - Onboard 10bit Wilkinson ADC
    - Continuous on-board digitization
      - “Floating point” Wilkinson ADC
  - Multiple front-ends
    - Varied input transistor parameters to determine optimal parameters for best noise performance

Prototype Performance

- Integrator
  - Performs as expected
  - Nominal gain 10mV/fC==10mV/6250e-
  - ==1mV/625e-
- Shaper stage
  - Programmable gain (2-10X)
    - Overall Sensitivity 62.5-313e-/mV
  - Programmable rise time output (50-500ns)
  - Programmable fall time determined by external resistor

Mux Output Performance

- Differential output
- Risetime of 30-40ns to 0.1% when driving a load of ~30pF
- Maximum output crosstalk <0.5%
  - More to be done on this, may depend on how the ADC load appears to the mux
  - More testing on this to be done in coordination with Harvard characterization of ADC

Noise Performance

- Noise measured using on-board ADC
- ADC works!
- Noise Simulations expect 150e-
  - 10pF detector capacitance
  - 250ns shaping time
  - 1us dual correlated sampling with onboard ADC
- Measured noise 154e- under same conditions on bench

Conclusions

- Device works!
- Future work
  - Test different input configurations to see if even better match is possible
  - Investigating packaging possibilities
    - With 32 inputs, a 128 pin package would allow connections for all modes to be brought out